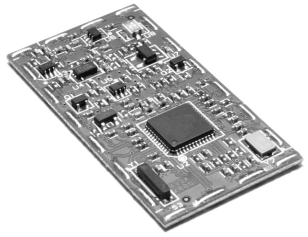
ZMN2405HP

High Power ZigBee Module

- ***2.4 GHz ZigBee Transceiver Module***
- ***Small Size, Light Weight, +18 dBm Transmitter Power***
- ***Sleep Current less than 3 µA***
- ***FCC and ETSI Certified for Unlicensed Operation***

The ZMN2405HP 2.4 GHz transceiver module is a low cost, high-power solution for point-to-point, point-to-multipoint and MESH wireless systems. The ZMN2405HP module provides the flexibility and versatility to serve applications ranging from cable replacements to sensor networks. Based on the IEEE 802.15.4 wireless standard and the ZigBee protocol stack, the ZMN2405HP module is easy to integrate and provides robust wireless communications including MESH network operation. The ZMN2405HP also includes Cirronet's powerful CSM application profile, which eliminates the need for customer firmware programming.



Shown with Shield Removed

ZMN2405HP Absolute Maximum Ratings

Rating	Value	Units
All Input/Output Pins	-0.3 to +3.6	V
Non-Operating Ambient Temperature Range	-40 to +85	°C

ZMN2405HP Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency Range			2405		2475	MHz
Operating Frequency Tolerance			-300		300	kHz
Spread Spectrum Method				Direct Sequence		
Modulation Type				O-QPSK		
Number of RF Channels				15		
RF Data Transmission Rate				250		kb/s
Symbol Rate Tolerance					120	ppm
RF Channel Spacing				5		MHz
Receiver Sensitivity, 10E-5 BER				-95		dBm
Upper Adjacent Channel Rejection, +5 MHz				41		dB
Lower Adjacent Channel Rejection, -5 MHz				30		dB
Upper Alternate Channel Rejection, +10 MHz				55		dB
Lower Alternate Channel Rejection, -10 MHz				53		dB
Maximum RF Transmit Power			16	17	18	dBm
Transmit Power Adjustment					20	dB
Optimum Antenna Impedance				50		Ω

ZMN2405HP Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
ADC Input Range			0		3.3	V
ADC Input Resolution			7		12	bits
ADC Input Impedance			55			MΩ
PWM Output Resolution					12	bits
UART Baud Rate			1.2		115.2	kb/s
Digital I/O:						
Logic Low Input Level			-0.3		0.5	V
Logic High Input Level			2.8		3.6	V
Logic Input Internal Pull-up/Pull-down Resistor			20			KΩ
GPIO3 Logic Low Sink Current					20	mA
Power Supply Voltage Range	V_{CC}		+3.3		+5.5	Vdc
Power Supply Voltage Ripple					10	mV_{P-P}
Receive Mode Current				33		mA
Transmit Mode Current				130		mA
Sleep Mode Current					3	µA
Operating Temperature Range			-40		85	°C

CAUTION: Electrostatic Sensitive Device. Observe precautions when handling.

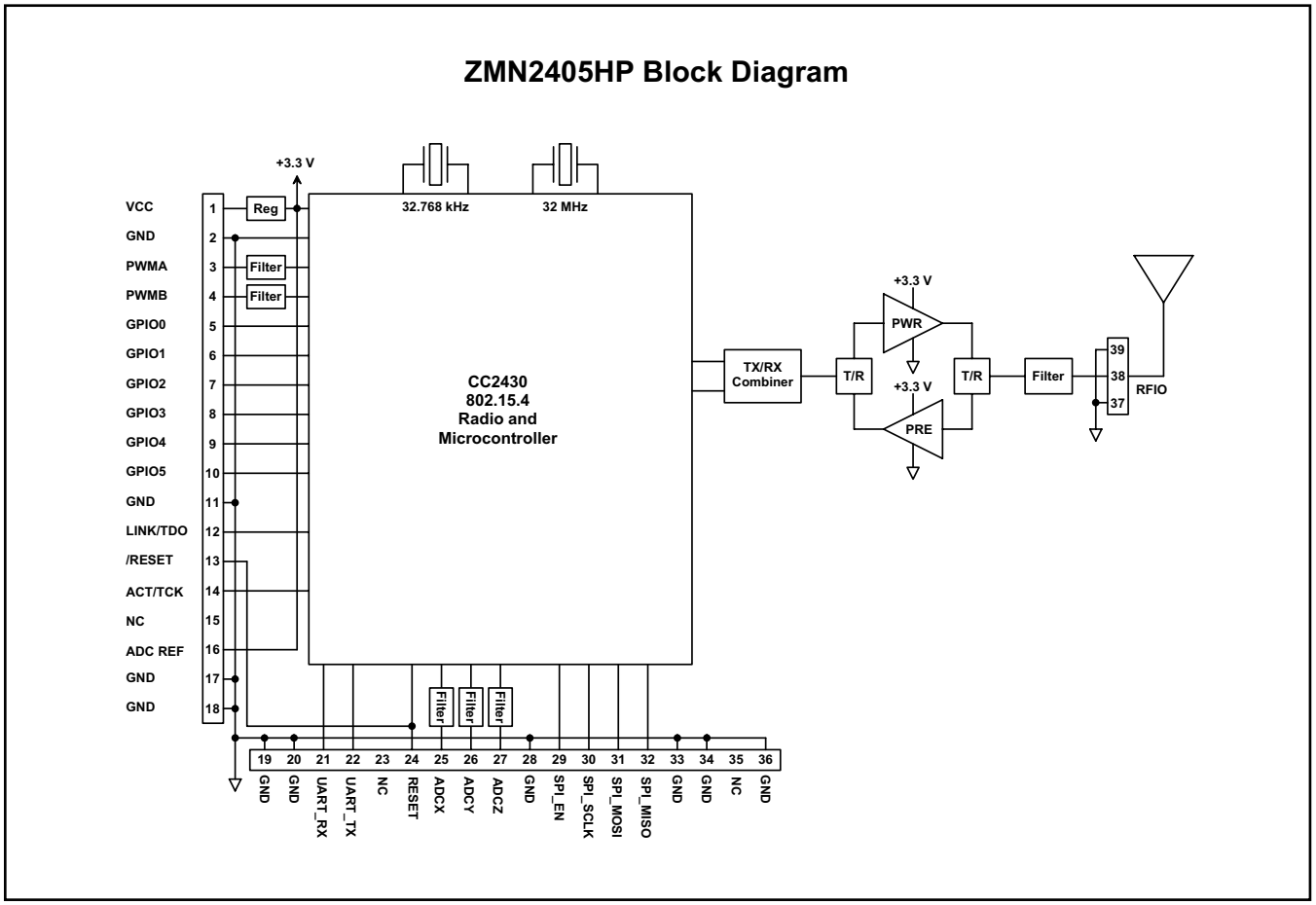


Figure 1

ZMN2405HP Hardware

The major hardware component of the ZMN2405HP is the CC2430 IEEE 802.15.4 compatible transceiver with integrated 8051 microcontroller. The ZMN2405HP operates in the frequency band of 2405 to 2475 MHz at a nominal output power of 63 mW.

The ZMN2405HP includes a low noise preamplifier in the receiver path and a power amplifier in the transmitter path, greatly increasing the operating range of the CC2430. Two crystals are provided to operate the CC2430, a 32 MHz crystal for normal operation and a 32.768 kHz crystal for precision sleep mode operation.

The ZMN2405HP provides a variety of application hardware interfaces including an SPI interface, UART interface, three 12-bit ADC inputs, two PWM (DAC) outputs, and six general purpose digital I/O ports.

ZMN2405HP Firmware

The main firmware components in the ZMN2405HP include the ZigBee protocol stack and the Cirronet Standard Module (CSM) application profile. The ZigBee protocol stack implements networking and security, with underlying support from the 802.15.4 Media Access Control (MAC) layer. The standard ZMN2405HP firmware implements a ZigBee full function device (FFD). This allows the module to operate as either a coordinator or router. Optional ZMN2405HP firmware is available that implements a ZigBee reduced function device (RFD). This allows the module to operate as an end device. The CSM profile provides an application programming interface (API) for all the ZMN2405HP application hardware interfaces. The CSM profile includes Network Discovery, Send/Receive Serial Data, Read/Write SPI Port, Read ADC Inputs, Write DAC Outputs, Read/Write GPIO and Module Configuration services. In addition, the CSM profile provides two sleep modes - timer sleep and interrupt sleep. See the *ZMN2405HP ZigBee Module Developer's Kit User's Manual* for complete details of the CSM profile API.

ZMN2405HP I/O Pad Descriptions

Pad	Name	Description
1	VCC	Power supply input, +3.3 to +5.5 Vdc.
2	GND	Power supply and signal ground. Connect to the host circuit board ground.
3	PWMA	Pulse-width modulated output A. Provides a DAC function when used with an external low-pass filter.
4	PWMB	Pulse-width modulated output B. Provides a DAC function when used with an external low-pass filter.
5	GPIO0	Configurable digital I/O port 0. When configured as an output, the power-on state is also configurable.
6	GPIO1	Configurable digital I/O port 1. When configured as an output, the power-on state is also configurable.
7	GPIO2	Configurable digital I/O port 2. When configured as an output, the power-on state is also configurable.
8	GPIO3	Configurable digital I/O port 3. When configured as an output, this high current port can sink up to 20 mA. The power-on output state is also configurable.
9	GPIO4	Configurable digital I/O port 4. When configured as an output, the power-on state is also configurable.
10	GPIO5	Configurable digital I/O port 5. When configured as an output, the power-on state is also configurable.
11	GND	Power supply and signal ground. Connect to the host circuit board ground.
12	LINK/DD	Output signal indicating module's link status in default mode. Also used by JTAG interface as Data Output.
13	/RESET	Active low hardware reset. Hold this input low when the power supply is below 2.7 V. In parallel with pad 24.
14	ACT/DC	Output signal indicating RF data activity. Also used by JTAG interface as Data Clock Input.
15	NC	No connection.
16	ADC REF	Module's +3.3 V regulated suppy, used for ratiometric ADC readings. Current drain on this output should be no greater than 5 mA.
17 - 20	GND	Power supply and signal grounds. Connect to the host circuit board ground.
21	UART_RX	Serial data input to UART.
22	UART_TX	Serial data output from UART.
23	NC	No connection.
24	/RESET	Active low hardware reset. Hold this input low when the power supply is below 2.7 V. In parallel with pad 13.
25	ADCX	7- to 12-bit ADC input X. ADC full scale can be referenced to +3.3 V supply or internal +2.5 V reference.
26	ADCY	7- to 12-bit ADC input Y. ADC full scale can be referenced to +3.3 V supply or internal +2.5 V reference.
27	ADCZ	7- to 12-bit ADC input Z. ADC full scale can be referenced to +3.3 V supply or internal +2.5 V reference.
28	GND	Power supply and signal ground. Connect to the host circuit board ground.
29	SPI_EN	Active-low enable output for SPI bus devices.
30	SPI_SCLK	SPI port clock signal.
31	SPI_MOSI	SPI port data output.
32	SPI_MISO	SPI port data input.
33-34	GND	Power supply and signal ground. Connect to the host circuit board ground.
35	NC	No connection.
36	GND	Power supply and signal ground. Connect to the host circuit board ground.
37	GND	RF ground. Connect to the host circuit board ground plane, and to shield when using coaxial cable.
38	RFIO	RF port. Connect the antenna to this port with a 50 Ω stripline or semi-rigid coaxial cable.
39	GND	RF ground. Connect to the host circuit board ground plane, and to shield when using coaxial cable.

RFIO Stripline

The RFIO pad on the radio module is connected directly to an antenna on the host circuit board, or to an MMCX or similar RF connector. It is important that this connection be implemented as a 50 ohm stripline. Referring to Figure 3, the width of this stripline depends on the thickness of the circuit board between the stripline and the

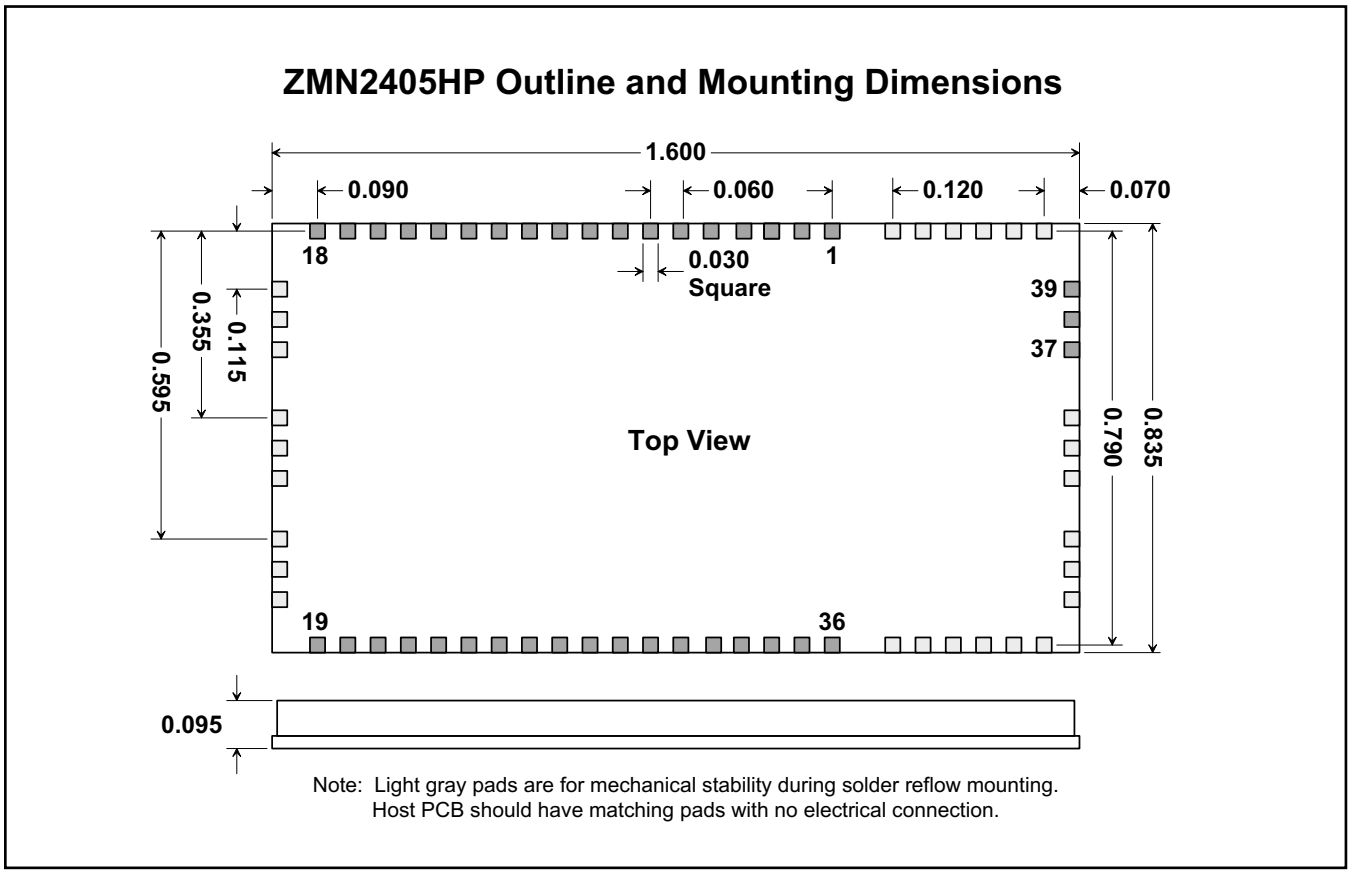


Figure 2

groundplane. For FR-4 type circuit board materials (dielectric constant of 4.7), the width of the stripline is equal to 1.75 times the thickness of the circuit board. Note that other circuit board traces should be spaced away from the stripline to prevent signal coupling, as shown in Figure 4. The stipline trace should be kept short to minimize its insertion loss.

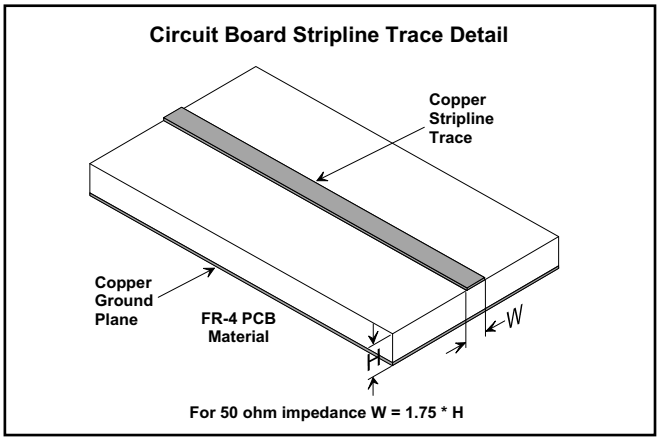


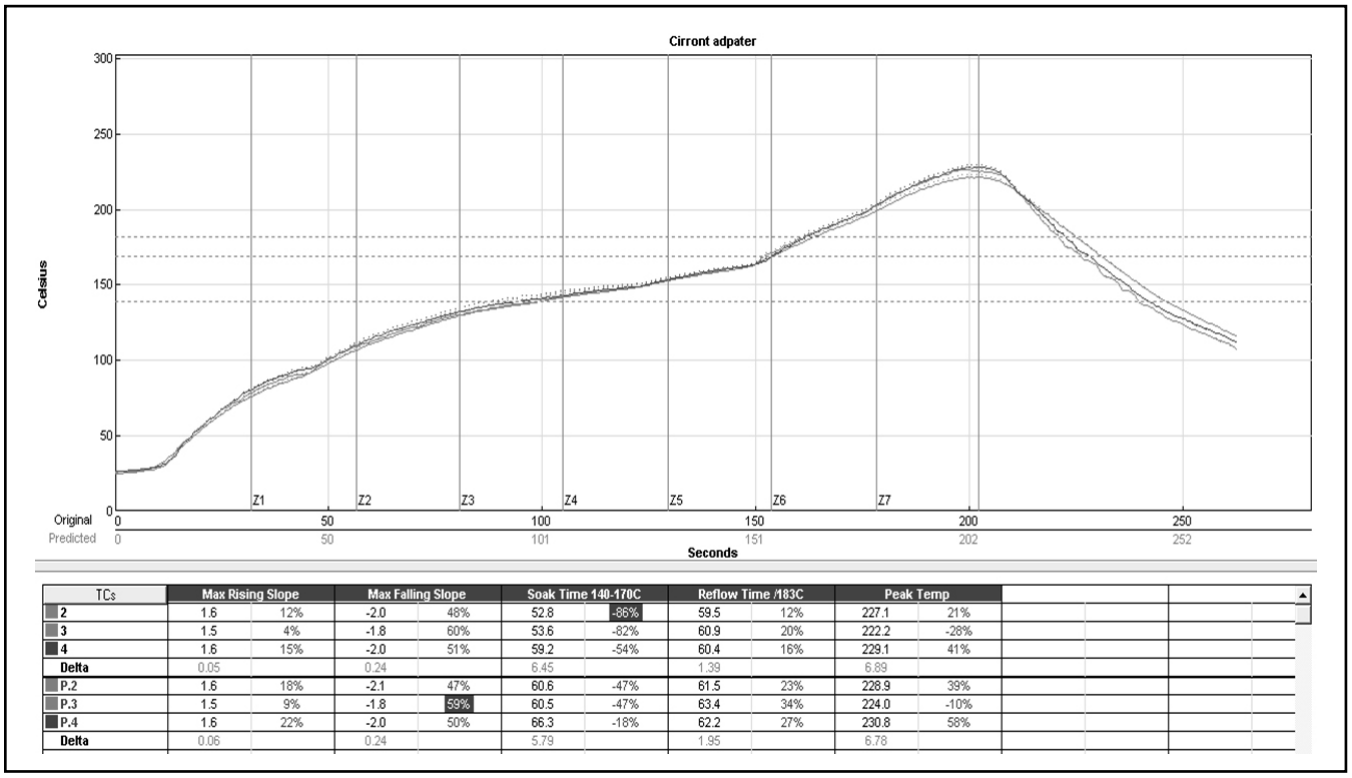
Figure 3

Trace Separation from 50 Ohm Microstrip	Length of Trace Run Parallel to Microstrip
100 mil	125 mil
150 mil	200 mil
200 mil	290 mil
250 mil	450 mil
300 mil	650 mil

Figure 4

Reflow Profile

An example solder reflow profile for mounting the radio module on its host circuit board is shown in Figure 5.



TCs	Max Rising Slope		Max Falling Slope		Soak Time 140-170C		Reflow Time /183C		Peak Temp	
2	1.6	12%	-2.0	48%	52.8	-86%	59.5	12%	227.1	21%
3	1.5	4%	-1.8	60%	53.6	-82%	60.9	20%	222.2	-28%
4	1.6	15%	-2.0	51%	59.2	-54%	60.4	16%	229.1	41%
Delta	0.05		0.24		6.45		1.39		6.89	
P.2	1.6	18%	-2.1	47%	60.6	-47%	61.5	23%	228.9	39%
P.3	1.5	9%	-1.8	59%	60.5	-47%	63.4	34%	224.0	-10%
P.4	1.6	22%	-2.0	50%	66.3	-18%	62.2	27%	230.8	58%
Delta	0.06		0.24		5.79		1.95		6.78	

Figure 5

Note: Specifications subject to change without notice.

file: zmn2405hp 02.vp, 2007.10.28 rev